SiGe-Power Amplifiers in Flipchip and Packaged Technology

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***Abstract* — A SiGe HBT with 22 GHz ft was optimized for power applications. A driver stage measured on wafer achieves Psat=23 dBm at 1.8 GHz with PAE up to 68%.**

A family of SiGe power amplifiers was developed for assembly in standard PSSOP packages and in flipchip technology. There are single and dualband PAs for 900 MHz and 1800 MHz GSM bands. The PAs are fully integrated three stage devices and feature high gain, output power and power added efficiency. The ICs incorporate power control circuits and operate from one positive supply voltage which can be as low as 2.5V.

At a nominal operating voltage of 3.5 V the 900 MHz packaged amplifier delivers up to 35 dBm output power at 58% PAE. The 1800 MHz amplifier produces up to 33 dBm power at 48% PAE. The devices can survive 5V supply voltage under full power. An optimized application design gives similar results for packaged and flipchip devices.

I. Introduction

The continuing growth of the mobile communication market generates a strong demand for low cost devices for handsets. TX and RX functions are already available in silicon with a high integration level. The PAs, which have a strong influence on the talk time of the phone, are traditionally implemented in GaAs [1, 2] to get a good PAE or in Si-LDMOS [3] to get the price down. SiGe heterobipolar transistors have the potential for high complexity integration combined with high efficiency operation up to several GHz at attractive costs [4].

Flipchip assembly has some advantages compared to conventional packaging techniques. At high operation frequencies (above 1 GHz) combined with power levels of more than 1 Watt, bond wires have strong influence on the amplifier performance because of the low output impedance of the PA. Solder balls, however, have very low inductance both for signal and ground connections. The required board space for a FC circuit is smaller than for a conventionally packaged device. On the contrary wire bonding allows more flexibility and if the exact RF behavior of the bond wires is known, similar performance is possible as packaged devices.

II. Technology for Power HBTs

The SiGe HBTs and the complete power amplifiers were fabricated using Atmel Wireless & Microcontrollers' (formerly TEMIC Semiconductors) bipolar SiGe1 production line. A detailed process description is given in [5, 6]. In addition to the npn-Transistors the process offers also lateral pnp-transistors for low power control functions. The passive elements R-L-C are all available in the technology. The resistors have three different sheet resistivities. Nitride capacitors and spiral inductors can be used to form on chip matching networks.

We compared different layouts for the active cell to get an optimum power HBT. Therefore the basic transistor as well as the grouping of the cells was varied. The collector thickness was adjusted for a break down voltage BV_{CE0}=7 V and a f_T around 22 GHz.

The large power devices required a careful layout to get good grounding, equal power distribution and low losses in the distribution network. The block size is limited by the current density in the collector wiring. Emitter ballast resistors prevent thermal runaway.

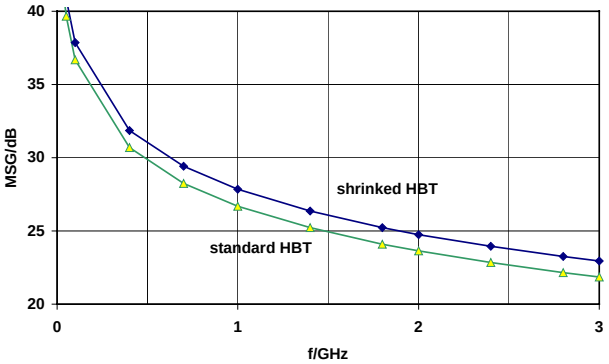

Fig. 1. MSG of shrinked driver HBT is 1dB higher than standard version.

For the PA development, two 10 and 20 finger devices in standard and shrinked pitch were measured on wafer with GSG probes. Transit frequency f_T peaks at 21.2 and 20.7 GHz for the standard 10 and 20 emitter devices while the shrinked versions reach 22.2 and 21.4 GHz. The MSG

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of the shrinked versions is 1 dB higher than that of the standard cell (Fig. 1). A small signal equivalent circuit [7, 8] shows a 20% reduction in Ccb while most other parameters remain unchanged.

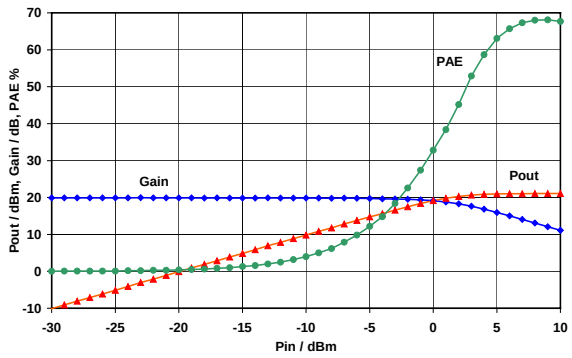

Fig. 2. Power sweep of driver HBT under maximum PAE load pull condition, f=1800 MHz.

Load-pull measurements of a driver stage HBT show a saturated output power of 23 dBm at 1.8 GHz. The PAE reaches 68% at optimum load (Fig. 2).

III. FLIPCHIP PROCESS

The finished silicon wafer is thinned to 450 µm thickness. A NiAu under bump metallization is formed by chemical deposition. For prototypes eutectic PbSn solder balls are picked and placed onto the wafer (Fig. 3). In waferscale production the balls are screen printed. Thickness and print shapes of the screen control the amount of the deposited solder. A reflow process forms the final solder balls (Fig. 5).

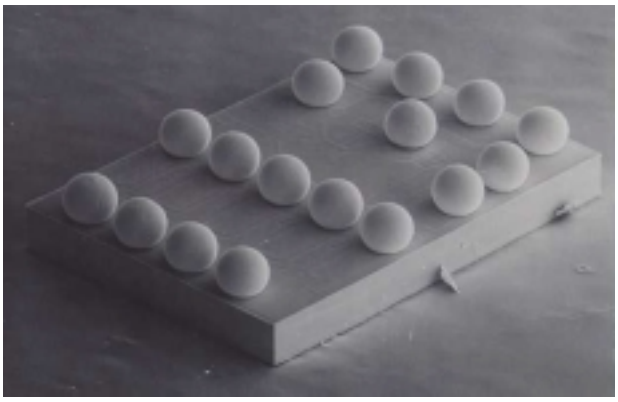

Fig. 3. Singleband flipchip die with solder balls

Ball size and pitch are a compromise between easy die attach and chip size. We used a diameter of 220 µm and a minimum pitch of 400 µm, which leads to relaxed design rules for the board layout. Most SMD assembly machines can handle these dimensions. However, it is possible to fabricate flipchips with down to 80 µm balls and 120 µm pitch.

The electrical effect of the bumps was calculated with electromagnetic simulation [10,11,12]. Ansofts HFSS was used to evaluate the 3D ball arrangement of the PA output stage.

The heat generated in the PA flows through the bumps to the board. The silicon substrate distributes the heat to every ball due to its good thermal conductivity. If there is enough space available, additional thermal bumps can be placed.

IV. PA DESIGN

A family of PAs was designed both for 900 MHz and 1800 MHz GSM operation. There are two versions, one for a standard PSSOP package and one for flipchip assembly. Besides the singleband PAs there is also a dualband PA with control logic for band switching (Fig. 4). Each PA has three RF-stages. The interstage matching circuits are on chip while the input and output matching is partly off chip. An integrated control circuit reduces the current consumption to less than 10 µA at power down without the need for external high-side switches.

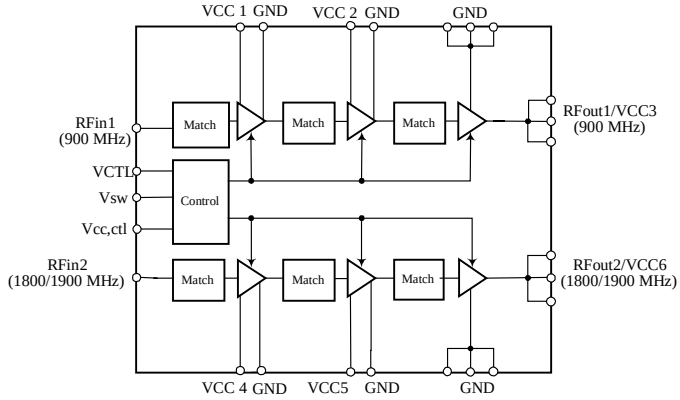

Fig. 4. Dualband power amplifier schematic.

The layout of the amplifiers in flipchip is slightly larger than the conventionally packaged counterparts, because of the additional space required for the solder balls. The dualband flipchip PA is shown in Fig. 5. The singleband PAs give more flexibility to the designer, because the 900 MHz and 1800 MHz sections can be handled separately.

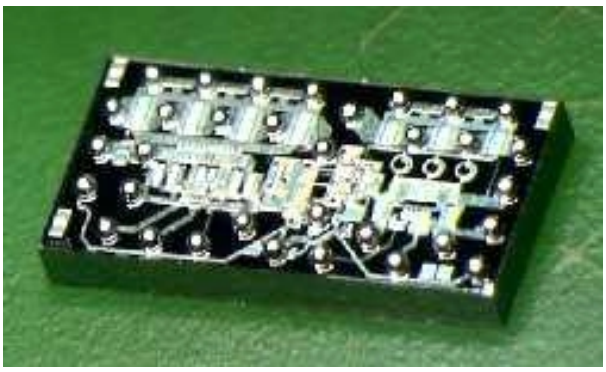

Fig. 5. Die photo of the dualband flipchip PA.

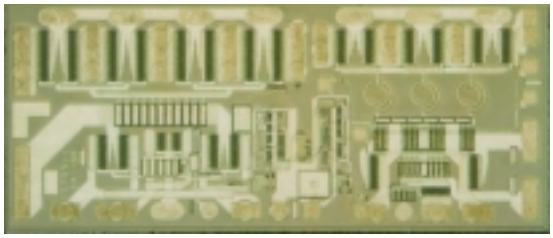

Fig. 6. Die photo of the dualband PA for assembly in a PSSOP package with bond wires.

V. PA Measurements

The PAs are soldered to an application board. The peripheral SMD components for input and output matching as well as the blocking capacitors are attached simultaneously by reflow soldering.

The packaged PAs, having three stages fully integrated, revealed at an operating voltage of 3.5 V an output power of 35 dBm at 900 MHz and 32.6 dBm at 1750 MHz with an associated PAE of 58% and 48% respectively (Fig. 8, 10). The supply voltage can range from 2.5 to 5 V with only minor degradation in PAE in the upper range. The PA delivers 2 dB more power at 5 V compared to the operation at 3.5 V.

The first cut of the flipchip PA on a special application board produces Pout=34.8 dBm with PAE 54% without final optimization (Fig. 9). This is close to the packaged version. With proper tuning we expect to exceed the measurements of the packaged devices.

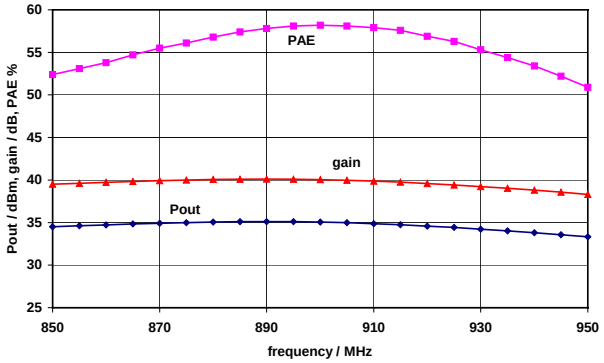

Fig. 8. Output power, gain and PAE of the 900 MHz PA in PSSOP package.

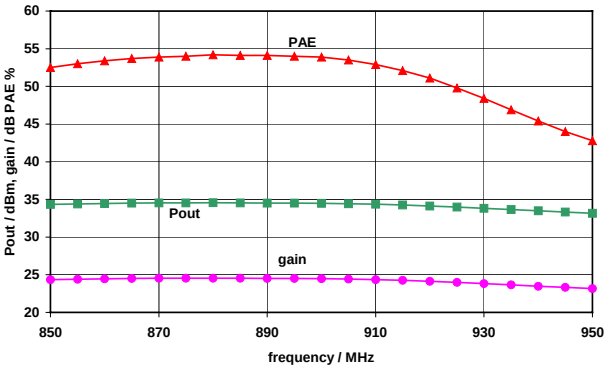

Fig. 9. Output power, gain and PAE of the 900 MHz flipchip PA.

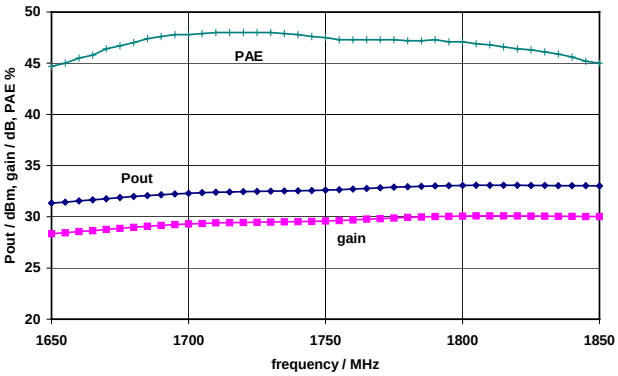

Fig. 10. Output power, gain and PAE of the 1800 MHz PA in PSSOP package.

VI. Conclusion

We realized a family of power amplifiers in SiGe HBT technology for the mobile handset market. After careful optimization of the SiGe power HBT, the performance is comparable to GaAs circuits. The amplifiers operate from

one positive supply voltage in a wide range. The flipchip devices show similar performance compared to conventionally bonded devices, but they need less board space.

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